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Signetics

PLS100/PLS101
Field-Programmable Logic Array (16 × 48 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 28**

DESCRIPTION

The PLS100 (Tri-state) and PLS101 (Open Collector) are bipolar, fuse Programmable Logic Arrays (FPLAs). Each device utilizes the standard AND/OR/Invert architecture to directly implement custom sum of product logic equations.

Each device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The True, Complement, or Don't Care condition of each of the 16 inputs can be ANDed together to comprise one P-term. All 48 P-terms can be selectively ORed to each output.

The PLS100 and PLS101 are fully TTL compatible, and chip enable control for expansion of input variables and output inhibit. They feature either Open Collector or Tri-state outputs for ease of expansion of product terms and application in bus-organized systems.

Order codes are contained on the pages following.

FEATURES

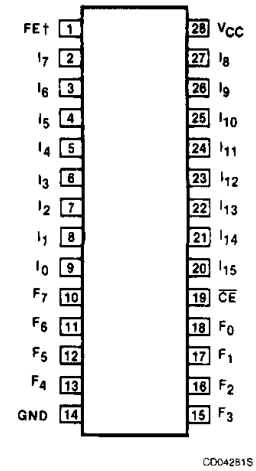
- **Field-Programmable (Ni-Cr link)**
- **Input variables: 16**
- **Output functions: 8**
- **Product terms: 48**
- **I/O propagation delay: 50ns (max.)**
- **Power dissipation: 600mW (typ.)**
- **Input loading: −100μA (max.)**
- **Chip Enable input**
- **Output option:**
  - **PLS100: Tri-state**
  - **PLS101: Open-Collector**
- **Output disable function:**
  - **Tri-state: Hi-Z**
  - **Open-Collector: High**

APPLICATIONS

- **CRT display systems**
- **Code conversion**
- **Peripheral controllers**
- **Function generators**
- **Look-up and decision tables**
- **Microprogramming**
- **Address mapping**
- **Character generators**
- **Data security encoders**
- **Fault detectors**
- **Frequency synthesizers**
- **16-bit to 8-bit bus interface**
- **Random logic replacement**

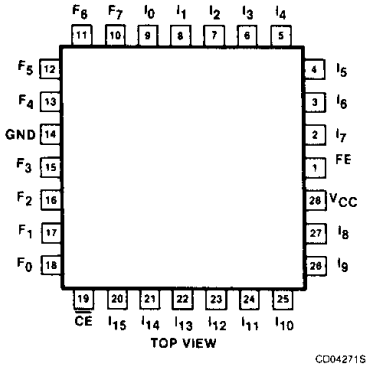
PIN CONFIGURATIONS

N Package



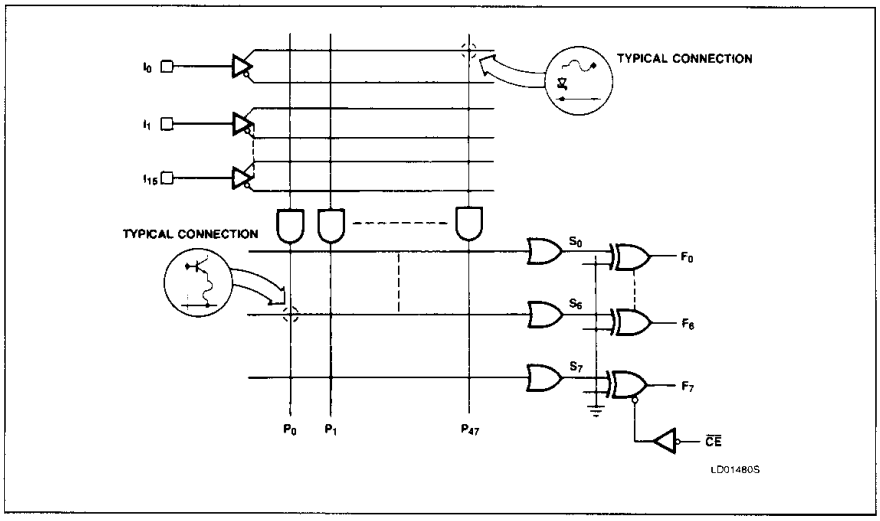
N = Plastic
†Open or grounded during normal operation.

A Package



A = Plastic Leaded Chip Carrier

FUNCTIONAL DIAGRAM



LOGIC FUNCTION

TYPICAL PRODUCT TERM:
$Pn = A \cdot \overline{B} \cdot C \cdot D \cdot \ldots$

TYPICAL LOGIC FUNCTION:
AT OUTPUT POLARITY = H
$Z = P0 + P1 + P2 \ldots$

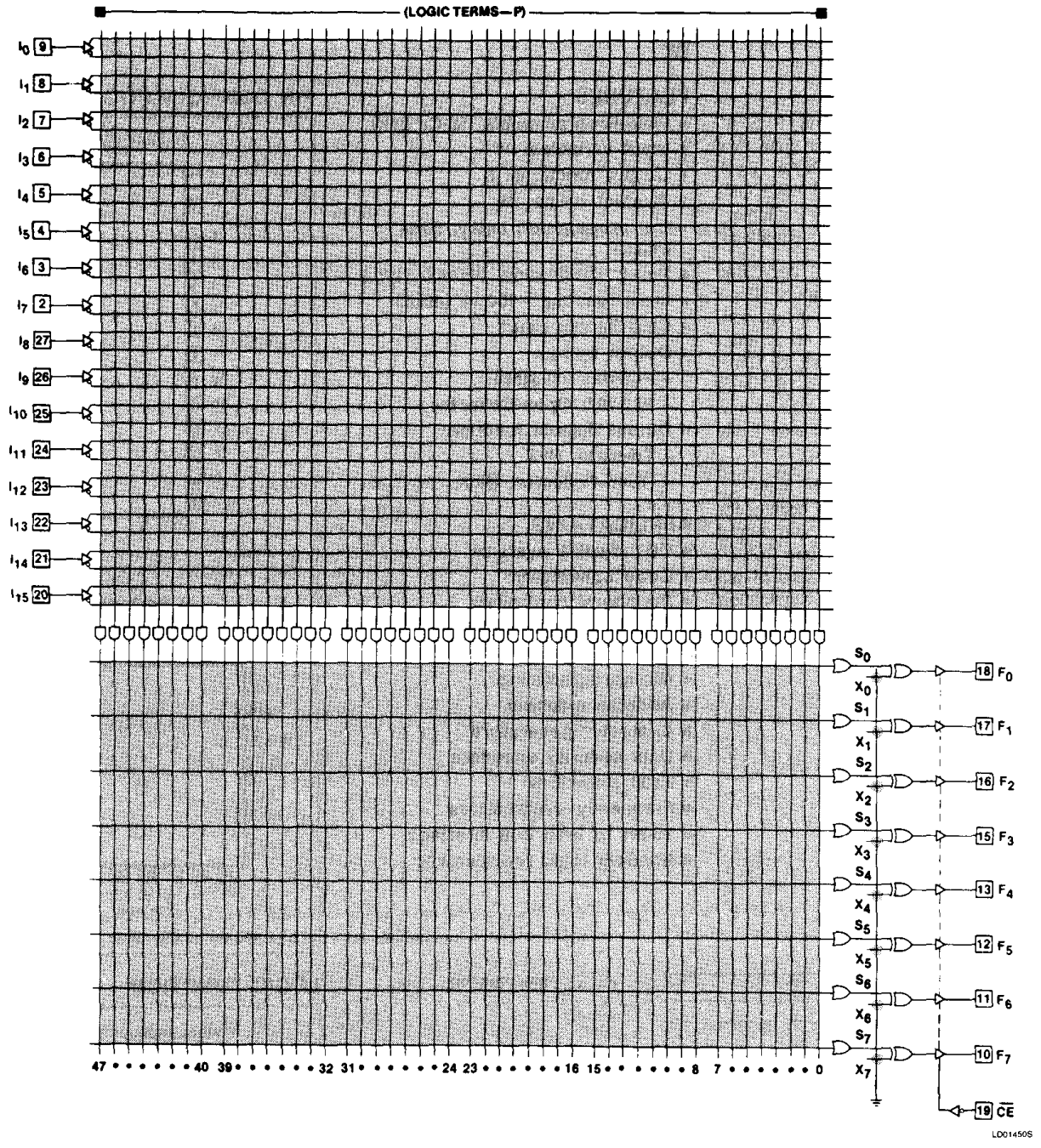
AT OUTPUT POLARITY = L
$Z = \overline{P0 + P1 + P2 + \ldots}$
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

NOTES:
1. For each of the 8 outputs, either function Z (Active-High) or $\overline{Z}$ (Active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I) and output pins (O).

Field-Programmable Logic Array (16 × 48 × 8)

PLS100/PLS101

FPLA LOGIC DIAGRAM



NOTES:
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ⊗ Programmable connection.

Field-Programmable Logic Array (16 × 48 × 8)

PLS100/PLS101

ORDERING INFORMATION

DESCRIPTION	TRI-STATE	OPEN-COLLECTOR
28-pin Plastic DIP 600mil-wide	PLS100N	PLS101N
28-pin Plastic Leaded Chip Carrier	PLS100A	PLS101A

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLS100 device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			
T_A	Operating	0	+75	°C
T_{STG}	Storage	−65	+150	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
Input voltage[3]						
V_{IH}	High	V_{CC} = Max	2			V
V_{IL}	Low	V_{CC} = Min			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	
Output voltage[3]						
V_{OH}	High (PLS100)[5]	V_{CC} = Min, I_{OH} = −2mA	2.4			V
V_{OL}	Low[6]	I_{OL} = 9.6mA		0.35	0.45	
Input current						
I_{IH}	High	V_{IN} = 5.5V		< 1	25	μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	
Output current						
$I_{O(OFF)}$	Hi-Z state (PLS100)	$\overline{CE}$ = High, V_{CC} = Max, V_{OUT} = 5.5V		1	40	μA
		V_{OUT} = 0.45V		−1	−40	
I_{OS}	Short circuit (PLS100)[4,7]	$\overline{CE}$ = Low, V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	170	mA
Capacitance						
C_{IN}	Input	$\overline{CE}$ = High, V_{CC} = 5.0V, V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		17		

Notes on following page.

Field-Programmable Logic Array (16 × 48 × 8)

PLS100/PLS101

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[2]	Max	
Propagation delay							
t_{PD}	Input	Output	Input		35	50	ns
t_{CE}	Chip enable	Output	Chip enable		15	30	ns
Disable time							
t_{CD}	Chip disable	Output	Chip enable		15	30	ns

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. All voltage values are with respect to network ground terminal.
4. Test one pin at a time.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied through a resistor to V_{CC}.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

Field-Programmable Logic Array (16 × 48 × 8)

PLS100/PLS101

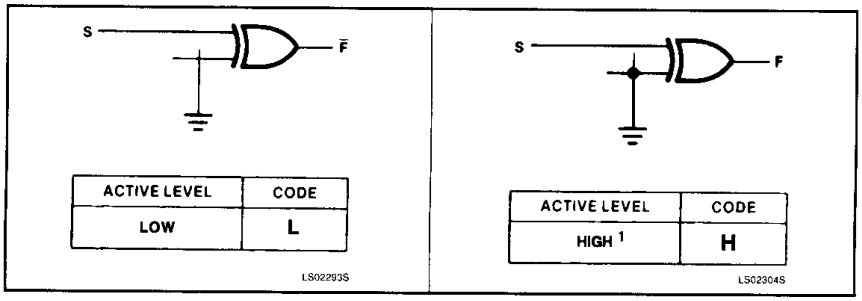
LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table.

In this Table the logic state or action of variables I, P, and F, associated with each Sum Term S_n, is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

OUTPUT POLARITY – (F)



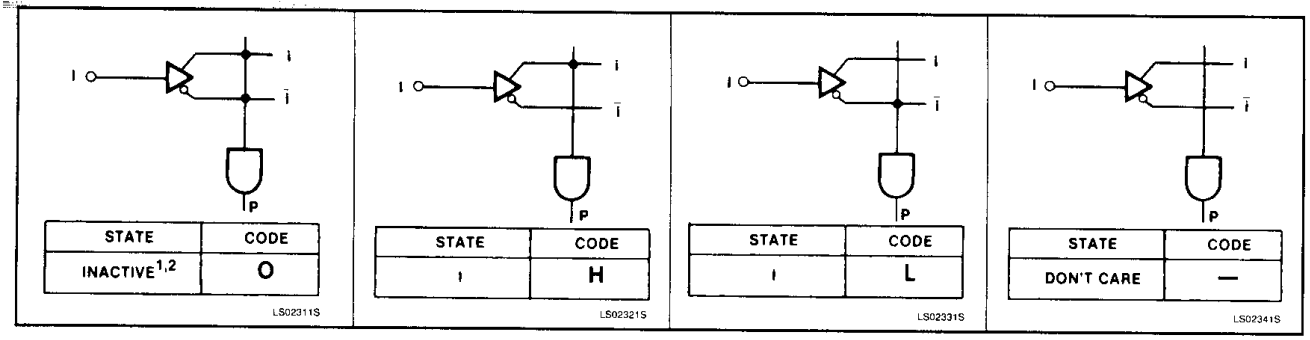
ACTIVE LEVEL	CODE
LOW	L

LS02293S

ACTIVE LEVEL	CODE
HIGH [1]	H

LS02304S

"AND" ARRAY – (I)



STATE	CODE
INACTIVE [1,2]	O

LS02311S

STATE	CODE
ı	H

LS02321S

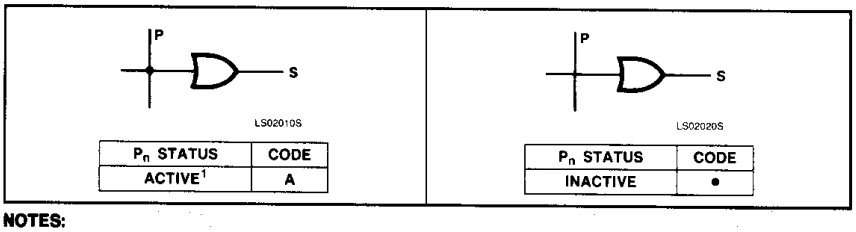
STATE	CODE
ı	L

LS02331S

STATE	CODE
DON'T CARE	—

LS02341S

"OR" ARRAY – (F)



LS02010S

P_n STATUS	CODE
ACTIVE [1]	A

LS02020S

P_n STATUS	CODE
INACTIVE	•

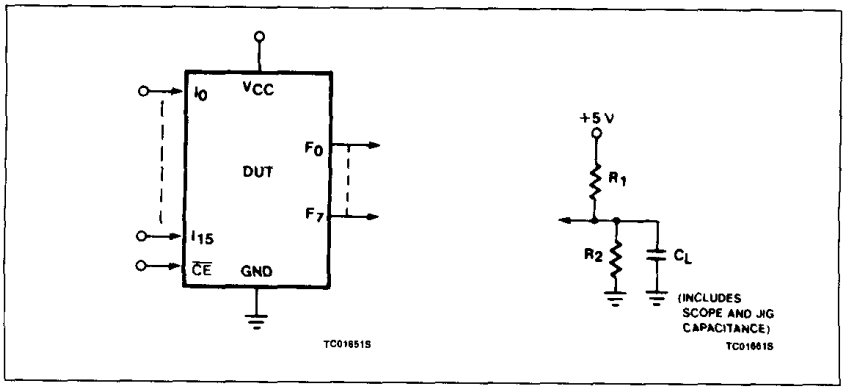
NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n.
2. Any gate P_n will be unconditionally inhibited if any one of its (I) link pairs is left intact.

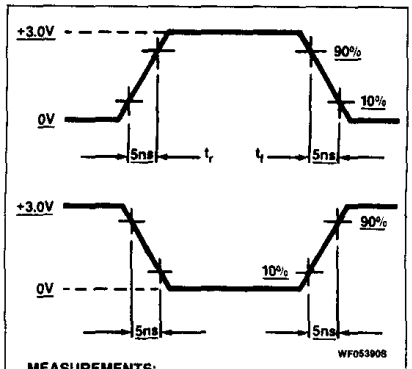
Field-Programmable Logic Array (16 × 48 × 8)

PLS100/PLS101

TEST LOAD CIRCUIT



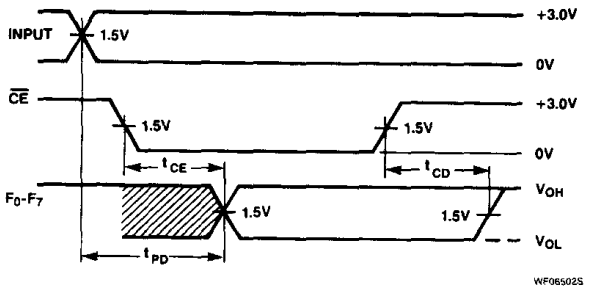
VOLTAGE WAVEFORM



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TIMING DIAGRAM



Read Cycle

TIMING DEFINITIONS

t_{CE}	Delay between beginning of Chip Enable low (with Input valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in off state (Hi-Z or High).
t_{PD}	Delay between beginning of valid Input (with Chip Enable Low) and when Data Output becomes valid.

VIRGIN STATE

The PLS100/101 virgin devices are factory shipped in an unprogrammed state, with all fuses intact, such that:

1. All P_n terms are disabled (inactive).
2. All P_n terms are active on all outputs.
3. All outputs are Active-High.

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PLS100/PLS101

FPLA PROGRAM TABLE

PROGAM TABLE ENTRIES

INPUT VARIABLE: Im (H) | Im (L) | Don't Care (—, dash)

OUTPUT FUNCTION: Prod. Term Present in F_P (A) | Prod. Term Not Present in F_P (• period)

OUTPUT ACTIVE LEVEL: Active High (H) | Active Low (L)

NOTES
1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

NOTE
Enter (—) for unused inputs of used P-terms

NOTES
1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____ CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ REV ____ DATE ____

	AND																POLARITY							
																	OR							
TERM	INPUT (I_m)																OUTPUT (F_P)							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
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PIN NO.	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9	10	11	12	13	15	16	17	18
VARIABLE NAME																								

TB01560S